

**What is claimed is:**

1           1.    A split gate flash memory cell, comprising:  
2           a substrate having a trench therein;  
3           a conductive layer disposed on the bottom of the  
4           trench;  
5           a pair of source regions, each disposed in the  
6           substrate adjacent to one sidewall of the  
7           trench and electrically connected by the  
8           conductive layer;  
9           a source isolation layer disposed on the conductive  
10          layer;  
11          a pair of tunnel oxide layers, respectively disposed  
12          on one sidewall of the trench and on the source  
13          isolation layer;  
14          a U-shaped floating gate having a plurality of  
15          inside tips disposed on the source isolation  
16          layer and contacting the tunnel oxide layers  
17          thereby;  
18          an inter-gate dielectric layer disposed on the U-  
19          shaped floating gate;  
20          a control gate disposed on the inter-gate  
21          dielectric;  
22          a conductive stud disposed on the control gate; and  
23          a drain region disposed in the substrate adjacent to  
24          the trench.

1           2.    The cell as claimed in claim 1, wherein a  
2           bottom insulating layer is further disposed under the  
3           conductive layer.

1           3.    The cell as claimed in claim 2, wherein the  
2           bottom insulating layer is silicon dioxide.

1           4.    The cell as claimed in claim 1, wherein the U-  
2           shaped floating gate and the control gate are N-type  
3           dopant doped polysilicon.

1           5.    The cell as claimed in claim 1, wherein the  
2           inter-gate dielectric layer is silicon dioxide.

1           6.    The cell as claimed in claim 1, wherein the  
2           conductive layer is N-type dopant doped polysilicon.

1           7.    The cell as claimed in claim 1, wherein the  
2           tunnel oxide layer is silicon dioxide.

1           8.    The cell as claimed in claim 1, wherein the  
2           conductive stud is N-type dopant doped polysilicon.

1           9.    The cell as claimed in claim 1, wherein a  
2           connecting oxide layer is further disposed between the U-  
3           shaped control gate and the inter-gate dielectric layer.

1           10.   The as claimed in claim 9, wherein the  
2           connecting oxide layer is silicon dioxide.

1           11.   The as claimed in claim 1, wherein the  
2           substrate is P-type silicon substrate.

1           12.   A method of fabricating split gate flash memory  
2           cells, comprising the steps of:

3           providing a substrate;

4           forming a plurality of parallel long trenches along  
5           a first direction in the substrate;

6 forming a conductive layer and a pair of source  
7 regions on the bottom of each long trench,  
8 wherein the source regions are respectively  
9 disposed in the substrate adjacent to two  
10 sidewalls of each long trench and electrically  
11 connected by the conductive layer therein;  
12 forming a source isolation layer on each conductive  
13 layer;  
14 forming a tunnel oxide on two sidewalls of each long  
15 trench;  
16 forming a U-shaped floating gate with a plurality of  
17 inside tips and a connecting oxide layer  
18 therein on each source isolation layer;  
19 forming an inter-gate dielectric layer on each U-  
20 shaped floating gate and the connecting oxide  
21 layer therein;  
22 forming a control gate on each inter-gate dielectric  
23 layer;  
24 forming a conductive stud on each control gate;  
25 forming a plurality of parallel shallow trench  
26 isolation (STI) regions along a second  
27 direction, defining a plurality of cell  
28 trenches; and  
29 forming a drain region in the substrate adjacent to  
30 each cell trench.

1 13. The method as claimed in claim 12, wherein the  
2 first direction is perpendicular to the second direction.

3 14. The method as claimed in claim 12, wherein the  
4 substrate is P-type silicon substrate.

1           15. The method as claimed in claim 12, further  
2 comprising before forming a plurality of parallel long  
3 trenches along a first direction in the substrate, the  
4 step of sequentially forming a pad oxide layer and a mask  
5 layer on the substrate.

1           16. The method as claimed in claim 15, wherein the  
2 mask layer is silicon nitride.

1           17. The method as claimed in claim 15, wherein the  
2 pad oxide layer is silicon dioxide.

1           18. The method as claimed in claim 12, further  
2 comprising before forming a conductive layer and a pair  
3 of source regions on the bottom of each long trench, the  
4 step of forming a bottom insulating layer on the bottom  
5 of each long trench.

1           19. The method as claimed in claim 12, wherein  
2 forming a conductive layer and a pair of source regions  
3 on the bottom of each long trench further comprises the  
4 steps of:

5           forming a source material layer in each long trench;  
6           performing a high temperature annealing process,  
7           driving out dopants in the source material  
8           layer, forming a pair of source regions in the  
9           substrate adjacent to two sidewalls of each  
10          long trench, electrically connected by the  
11          conductive layer therebetween; and

12          removing the source material layer from each long  
13          trench.

1           20. The method as claimed in claim 19, wherein the  
2 source material layer is N-type doped silicon dioxide.

1           21. The method as claimed in claim 20, wherein the  
2 N-type doped silicon dioxide comprises phosphorous (P)  
3 doped silicon dioxide or arsenic (As) doped silicon  
4 dioxide.

1           22. The method as claimed in claim 12, further  
2 comprising before forming a tunnel oxide on two sidewalls  
3 of each long trench, performing a threshold voltage  
4 implantation on the sidewalls of each long trench.

1           23. The method as claimed in claim 12, wherein  
2 forming a U-shaped floating gate with a plurality of  
3 inside tips and a connecting oxide layer therein on the  
4 source isolation layer further comprises:

5           conformably depositing a floating gate layer in each  
6           long trench;

7           forming a connecting oxide layer on the floating  
8           gate layer in each long trench;

9           removing portions of the floating gate layer exposed  
10           by the connecting oxide layer, forming a U-  
11           shaped floating gate with the connecting oxide  
12           layer therein;

13           forming a floating gate oxide spacer on sidewalls of  
14           each long trench;

15           forming a floating gate nitride spacer on the  
16           floating gate oxide spacer;

17           partially etching the connecting oxide, exposing  
18           part of the inside U-shaped floating gate;

19 isotropically etching the inside U-shaped floating  
20 gate, forming a plurality of tips on the  
21 insides thereof; and  
22 removing the floating gate oxide spacers, the  
23 floating gate nitride spacers, and part of the  
24 tunnel oxides adjacent to the sidewalls of each  
25 long trench, leaving a U-shaped floating gate  
26 with a plurality of inside tips and a  
27 connecting oxide layer therein.

1 24. The method as claimed in claim 23, wherein the  
2 method for partially etching the connecting oxide is wet  
3 etching.

1 25. The method as claimed in claim 12, further  
2 comprising before forming a conductive stud on the  
3 control gate, the step of forming control gate spacers on  
4 sidewalls of each long trench.

1 26. The method as claimed in claim 25, wherein the  
2 control gate spacer is silicon dioxide.

1 27. The method as claimed in claim 12, wherein  
2 forming a plurality of parallel shallow trench isolation  
3 (STI) regions along a second direction, and defining a  
4 plurality of cell trenches further comprises:

5 sequentially performing a photolithography process  
6 and an etching process, defining a plurality of  
7 parallel long isolation trenches along a second  
8 direction, stopping at the source isolation  
9 layer therein; and

forming an insulating layer in the long isolation  
trenches.

28. The method as claimed in claim 27, wherein the  
insulating layer is silicon dioxide.

29. The method as claimed in claim 27, wherein the  
method of forming the insulating layer is high density  
plasma enhanced chemically vaporization deposition (HDP  
CVD).

30. The method as claimed in claim 12, wherein  
forming a drain region in the substrate adjacent to each  
of the cell trenches further comprises:

removing the mask layer, exposing the pad oxide  
layer;

performing a drain implantation;

performing a thermal annealing process, forming a  
drain region in the substrate adjacent to each  
cell trenches;

removing the pad oxide layer; and

forming a second insulating layer on each drain  
region.

31. The method as claimed in claim 30, wherein  
impurities used in the drain region implantation are N-  
type impurities.

32. The method as claimed in claim 31, wherein the  
N-type impurities are phosphorous (P) ions or arsenic  
(As) ions.